CLAIMS

1. A transceiver connected to a data source and a data receiver, comprising:

an input port for accepting a control signal having a first and a second state;

a serializer designed to operate at a first data rate; and

a first interface that receives a first set of data from the data source at a second data rate and delivers a second set of data to the serializer at the first data rate, the second data rate being lower than the first data rate when the control signal is at the first state and the second rate being same as the first data rate when the control signal is at the second state.

2. The transceiver of claim 1 wherein the serializer is controlled by a reference clock signal, and wherein the first interface further comprises a circuit for generating a first clock signal based on the reference clock signal, the first clock signal being used by the data source to deliver the first set of data to the first interface, the first clock signal having a lower frequency than the reference clock signal when the control signal is at the first state.

3. The transceiver of claim 2 wherein the first clock signal has a frequency that is substantially equal to half of the reference clock.

4. The transceiver of claim 2 wherein the first interface further inserts additional bits in the first set of data to generate the second set of data.

5. The transceiver of claim 4 wherein the first interface replicates every bit in the first set of data to generate the second set of data.

6. The transceiver of claim 1 further comprising:

a deserializer designed to operate at the first data rate; and

a second interface that receives a third set of data from the deserializer at the first data rate and delivers a fourth set of data to the data receiver at the second data rate.

7. The transceiver of claim 6 wherein the deserializer recovers a clock signal, and wherein the second interface further comprises a circuit that generates a second clock signal based on the recovered clock signal, the second clock signal being used by the data receiver to receive the fourth set of data.

8. The transceiver of claim 7 wherein the second clock signal has a frequency that is lower than that of the recovered clock signal when the control signal is at the first state.

9. The transceiver of claim 8 wherein the second clock signal has a frequency that is substantially equal to half of the recovered clock signal.

10. The transceiver of claim 6 wherein the second interface further removes bits in the third set of data to generate the fourth set of data when the control signal is at the first state.

11. The transceiver of claim 10 wherein the second interface removes every alternate bit in the third set of data to generate the fourth set of data.